CLAIMS

1. A low voltage sensing circuit for a non-volatile memory (NVM) device, the NVM device including a plurality of NVM cells including a first NVM cell coupled to a first bit line and a reference NVM cell coupled to a second bit line, wherein the low voltage sensing circuit comprises:

a first PMOS transistor having a first terminal connected to a system voltage source, a second terminal coupled to the first bit line, and a gate terminal;

a second PMOS transistor having a first terminal connected to the system voltage source, a second terminal coupled to the second bit line, and a gate terminal;

a comparator having a first input terminal and a second input terminal;

a first voltage source circuit connected between the second terminal of the first PMOS transistor and the first input terminal of the comparator; and

a second voltage source circuit connected between the second terminal of the second PMOS transistor and the second input terminal of the comparator.

2. The low voltage sensing circuit according to Claim 1, further comprising a first NMOS transistor having a first terminal connected to the second terminal of the first PMOS transistor, a second terminal coupled to the first bit line, and a gate terminal connected to a bias voltage source.

3. The low voltage sensing circuit according to Claim 2, wherein the first terminal of the first NMOS transistor is connected to a positive terminal of the first voltage source circuit.

4. The low voltage sensing circuit according to Claim 2, further comprising a second NMOS transistor having a first terminal connected to the second terminal of the second PMOS transistor, a second terminal coupled to the second bit line, and a gate terminal connected to the bias voltage source.

5. The low voltage sensing circuit according to Claim 4,

wherein the first terminal of the first NMOS transistor is connected to a positive terminal of the first voltage source circuit, and

wherein the first terminal of the second NMOS transistor is connected to a positive terminal of the second voltage source circuit.

6. A non-volatile memory (NVM) device comprising:

an array of NVM cells including a first NVM cell coupled to a first bit line and a reference NVM cell coupled to a second bit line; and

a low voltage sensing circuit for determining a programmed/erased state of the first NVM cell, the low voltage sensing circuit including:

a first PMOS transistor having a first terminal connected to a system voltage source, a second terminal coupled to the first bit line, and a gate terminal;

a second PMOS transistor having a first terminal connected to the system voltage source, a second terminal coupled to the second bit line, and a gate terminal;

a comparator having a first input terminal and a second input terminal;

a first voltage source circuit connected between the second terminal of the first PMOS transistor and the first input terminal of the comparator; and

a second voltage source circuit connected between the second terminal of the second PMOS transistor and the second input terminal of the comparator.

7. The NVM device according to Claim 6, wherein the low voltage sensing circuit further comprises a first NMOS transistor having a first terminal connected to the second terminal of the first PMOS transistor, a second terminal coupled to the first bit line, and a gate terminal connected to a bias voltage source.

8. The NVM device according to Claim 7, wherein the first terminal of the first NMOS transistor is connected to a positive terminal of the first voltage source circuit.

9. The NVM device according to Claim 7, wherein the low voltage sensing circuit further comprises a second NMOS transistor having a first terminal connected to the second terminal of the second PMOS transistor, a second terminal coupled to the second bit line, and a gate terminal connected to the bias voltage source.

10. The NVM device according to Claim 9,

wherein the first terminal of the first NMOS transistor is connected to a positive terminal of the first voltage source circuit, and

wherein the first terminal of the second NMOS transistor is connected to a positive terminal of the second voltage source circuit.

11. A low voltage sensing circuit for a non-volatile memory (NVM) device, the NVM device including a plurality of NVM cells including a first NVM cell coupled to a first bit line and a reference NVM cell coupled to a second bit line, wherein the low voltage sensing circuit comprises:

a first PMOS transistor having a first terminal connected to a system voltage source, a second terminal coupled to the first bit line, and a gate terminal;

a second PMOS transistor having a first terminal connected to the system voltage source, a second terminal coupled to the second bit line, and a gate terminal;

a comparator having a first input terminal connected to the gate terminal of the first PMOS transistor, and a second input terminal connected to the gate terminal of the second PMOS transistor;

a first source-follower circuit connected between the second terminal of the first PMOS transistor and the first input terminal of the comparator; and

a second source-follower circuit connected between the second terminal of the second PMOS transistor and the second input terminal of the comparator.

12. The low voltage sensing circuit according to Claim 11, further comprising a first NMOS transistor having a first terminal connected to the second terminal of the first PMOS transistor, a second terminal coupled to the first bit

line, and a gate terminal connected to a bias voltage source.

13. The low voltage sensing circuit according to Claim 12, wherein the first source-follower circuit comprises:

a current source having a first terminal connected to ground;

a second NMOS transistor having a first terminal connected to a second terminal of the current source and to the first input terminal of the comparator, a second terminal connected to the system voltage source, and a gate terminal connected to the first terminal of the first NMOS transistor.

14. The low voltage sensing circuit according to Claim 13, further comprising a third NMOS transistor having a first terminal connected to the second terminal of the second PMOS transistor, a second terminal coupled to the second bit line, and a gate terminal connected to the bias voltage source.

15. The low voltage sensing circuit according to Claim 14,

wherein the second source-follower circuit comprises:

a second current source having a first terminal connected to ground;

a fourth NMOS transistor having a first terminal connected to a second terminal of the second current source and to the second input terminal of the comparator, a second terminal connected to the system voltage source, and a gate terminal connected to the first terminal of the third NMOS transistor.

16. A non-volatile memory (NVM) device comprising:

an array of NVM cells including a first NVM cell coupled to a first bit line and a reference NVM cell coupled to a second bit line; and

a low voltage sensing circuit for determining a programmed/erased state of the first NVM cell, the low voltage sensing circuit including:

a first PMOS transistor having a first terminal connected to a system voltage source, a second terminal coupled to the first bit line, and a gate terminal;

a second PMOS transistor having a first terminal connected to the system voltage source, a second terminal coupled to the second bit line, and a gate terminal;

a comparator having a first input terminal connected to the gate terminal of the first PMOS transistor, and a second input terminal connected to the gate terminal of the second PMOS transistor;

a first source-follower circuit connected between the second terminal of the first PMOS transistor and the first input terminal of the comparator; and

a second source-follower circuit connected between the second terminal of the second PMOS transistor and the second input terminal of the comparator.

17. The NVM device according to Claim 16, wherein the low voltage sensing circuit further comprises a first NMOS transistor having a first terminal connected to the second terminal of the first PMOS transistor, a second terminal coupled to the first bit line, and a gate terminal connected to a bias voltage source.

18. The NVM device according to Claim 17, wherein the first source-follower circuit comprises:

a current source having a first terminal connected to ground;

a second NMOS transistor having a first terminal connected to a second terminal of the current source and to the first input terminal of the comparator, a second terminal connected to the system voltage source, and a gate terminal connected to the first terminal of the first NMOS transistor.

19. The NVM device according to Claim 18, wherein the low voltage sensing circuit further comprises a third NMOS transistor having a first terminal connected to the second terminal of the second PMOS transistor, a second terminal coupled to the second bit line, and a gate terminal connected to the bias voltage source.

20. The low voltage sensing circuit according to Claim 19,

wherein the second source-follower circuit comprises:

a second current source having a first terminal connected to ground;

a fourth NMOS transistor having a first terminal connected to a second terminal of the second current source and to the second input terminal of the comparator, a second terminal connected to the system voltage source, and a gate terminal connected to the first terminal of the third NMOS transistor.